5A Peak Current Dual Channels Low Side Gate DriverGENERAL

DESCRIPITION

The MX27524 is a dual, high current, low side gate driver. Each of the two outputs is capable of sourcing and sinking 5A peak current, and has a maximum voltage rating of 20V. Each channel has dual independent enable pins that default to ON if not connected. Fast propagation delay times and fast rise and fall times make the MX27524 well suited for high frequency applications.

In addition, the drivers feature matched internal propagation delays between A and B channels for applications requiring dual gate drivers with critical timing, such as synchronous rectifier.

FEATURES

♦Two independent drivers, each capable of sourcing and sinking 5A

♦CMOS and TTL compatible inputs

♦Independent enable for each channel

♦4.5V to 20V supply voltage range

♦-40℃ to +125℃ extended operating temperature range

♦±4kV ESD rating (Human Body Model)

♦Thermally enhanced 8-pin MSOP package and standard 8-pin SOP package

♦Internal under voltage lockout circuitry

♦Fast INX propagation delays (15ns typical)

♦Fast rise and fall times (7ns typical and 1.8nF load)

♦Propagation delay matching (5ns MAX)

♦These are Pb-free device

Battery management systems

APPLICATIONS

Pulse laser for distance test

DC-DC converters

Motor controllers

Power inverters

Synchronous rectifier circuits

GENERAL INFORMATION

Ordering information	
Part Number	**Description**
MX27524ES	eMSOP8/Exposed Thermal Pad
MX27524S	SOP8

Package dissipation rating	
Package	**RθJA（℃/W）**
eMSOP8	60
SOP8	130

Absolute maximum ratings	
Parameter	**Value**
VCC DC supply voltage	-0.3 to 26V
ENA/ENB pins	-0.3 to VCC+0.3V
INA/INB pins	-0.3 to VCC+0.3V
OUTA/OUTB pins（pulse <200ns）	-2.0 to VCC+0.3V
Junction temperature	-40 to 125℃
Storage temperature T_{STG}	-55 to 150℃
Leading temperature（soldering, 10secs）	260℃
ESD Susceptibility HBM	±4000V

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device

Recommended operating condition		
Symbol	**Parameter**	**Range**
VCC	VCC supply voltage	4.5-20V
EN/IN	ENA/ENB/INA/INB	-0.3-VCC
OUT	Repetitive Pulse < 200ns	-2.0-VCC

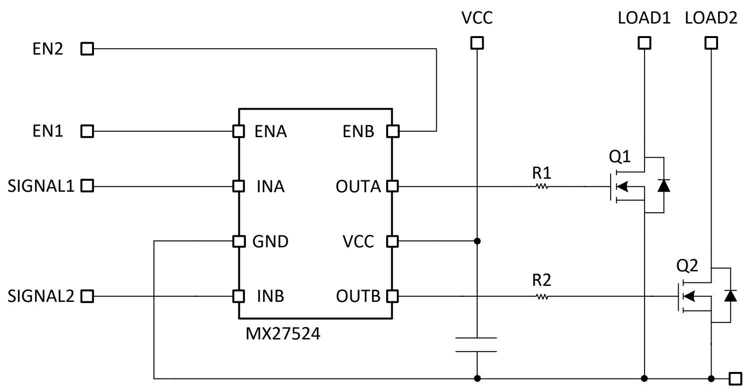


Figure1 MX27524 application for two channels

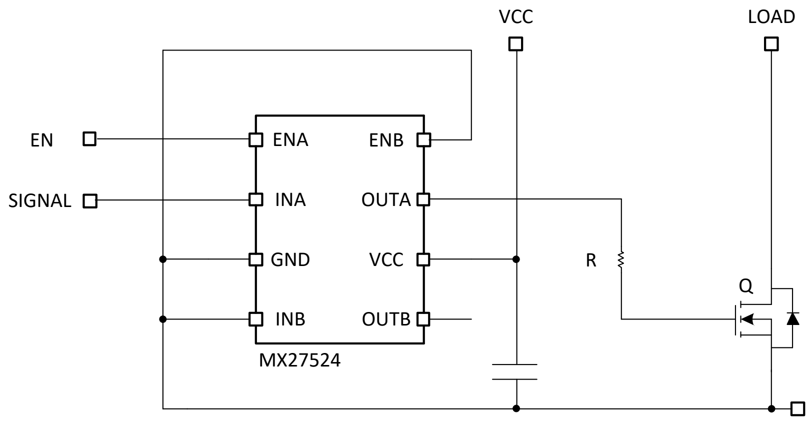


Figure2 MX27524 application for one channel

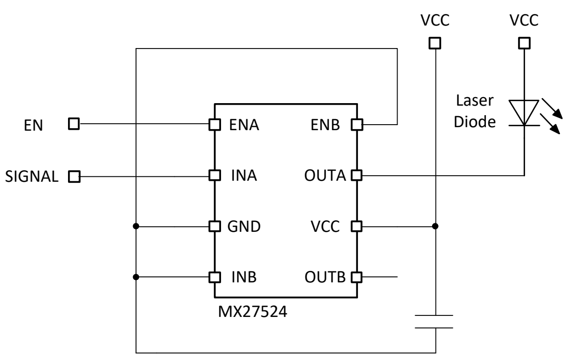


Figure3 MX27524 application for laser distance test

TERMINAL ASSIGMENTS

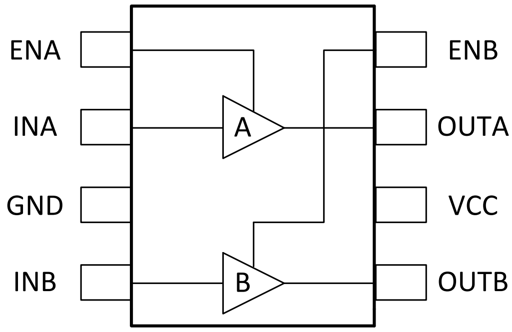


Figure4 pin information

PIN NO.	PIN name	Description
1	**ENA**	Enable input for channel A. A logic high enables channel A (the state of OUTA is determined by INA). A logic low disables OUTA (OUTA held low regardless of INA). Floating is logic high internal.
2	**INA**	Channel A logic input. Internally pulled to GND.
3	**GND**	Ground. Common ground reference for the device.
4	**INB**	Channel B logic input. Internally pulled to GND.
5	**OUTB**	Channel B output, capable of sourcing and sinking 5A
6	**VCC**	Supply voltage.
7	**OUTA**	Channel A output, capable of sourcing and sinking 5A
8	**ENB**	Enable input for channel B. A logic high enables channel B (the state of OUTB is determined by INB). A logic low disables OUTB (OUTB held low regardless of INB). Floating is logic high internal.
The thermal pad on the bottom of the thermally enhanced device, MX27524ES, may be connected to GND or left floating; it must not be connected to any other net. The thermal pad is not intended to carry current.		

BLOCK DISGRAM

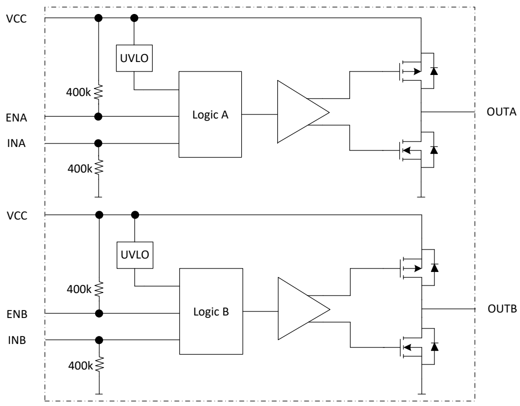
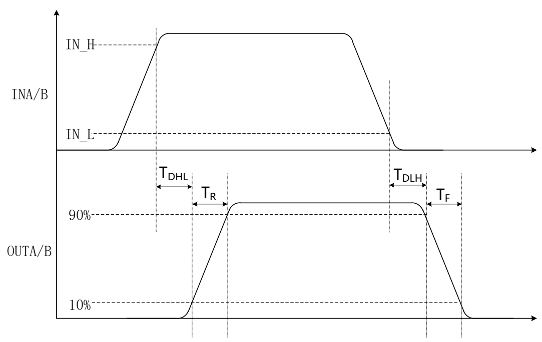


Figure5 block diagram

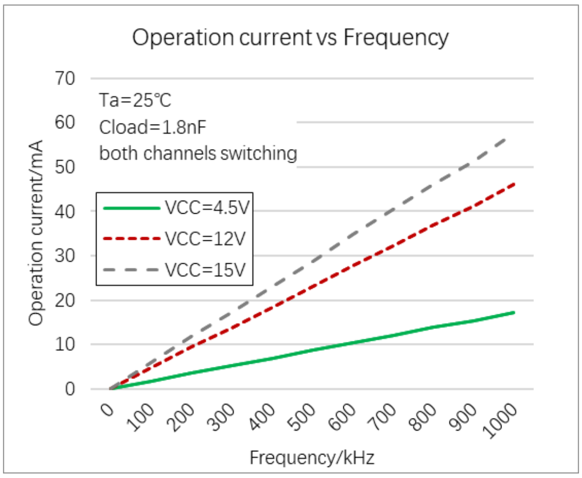
Electrical characteristics

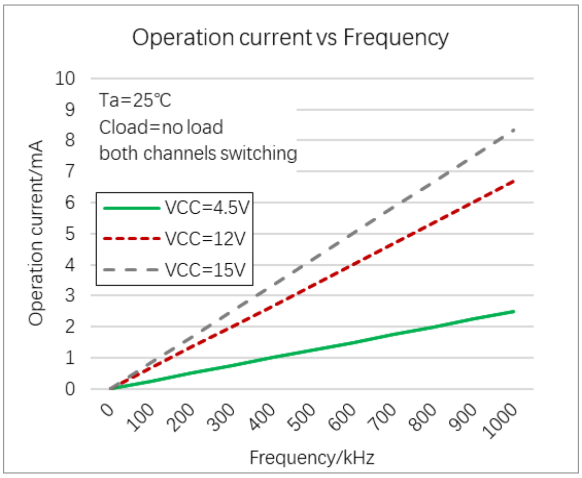
SUPPLY		（TA=25℃，VCC=12V, unless otherwise noted）				
Symbol	**Parameter**	**Test condition**	**Min**	**Typ.**	**Max**	**Unit**
I_{CC}	Supply current，VCC=12V	OUT and OUTB open		1.0	2.5	mA
I_{CC_OFF}	VCC=3.0V, INA=INB=VCC			80	120	μA
	VCC=3.0V, INA=INB=GND			60	100	μA
Under Voltage Lockout (UVLO)						
U_{VLO_ON}	UVLO rising threshold	VCC rising	3.1	3.3	3.5	V
U_{VLO_OFF}	UVLO falling threshold	VCC falling	3.5	3.85	4.2	V
U_{VLO_HYS}	UVLO threshold hysteresis		0.2	0.5	0.8	V
Logic inputs (INA, INB, ENA, ENB)						
V_{IN_L}	Input logic low		0.9	1.2	1.5	V
V_{IN_H}	Input logic high		1.8	2.1	2.4	V
V_{EN_L}	Enable logic low		0.85	1.1	1.35	V
V_{EN_H}	Enable logic high		1.75	2.05	2.35	V
R_{ENH}	Input pull up resistor			400k		ohm
R_{INL}	Input pull down resistor			400k		ohm
Output drivers (OUTA, OUTB)						
R_OH	Output pull up resistance	IOUT=-10mA, TJ=25℃		0.8	1.3	ohm
		IOUT=-10mA		1.0	1.5	ohm
R_OL	Output pull down resistance	IOUT=10mA, TJ=25℃		0.6	1.1	ohm
		IOUT=10mA		0.8	1.4	ohm
$I_{SOUPEAK}$	High level output current			5.0		A
$I_{SNKPEAK}$	Low level output current			-5.0		A
T_{RISE}	Rise time	CLOAD=1.8nF		7	15	ns
T_{FALL}	Fall time	CLOAD=1.8nF		7	15	ns
T_{DLH}	Propagation delay, Low to High	CLOAD=1.8nF	5	15	25	ns
T_{DHL}	Propagation delay, High to Low	CLOAD=1.8nF	5	15	25	ns
T_{MATCH}	Propagation delay matching		-5		5	ns

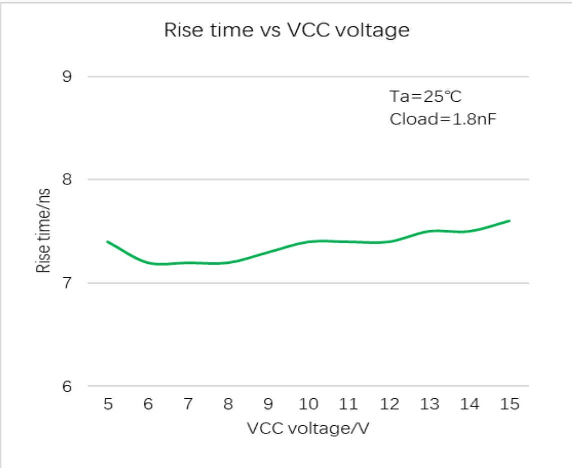


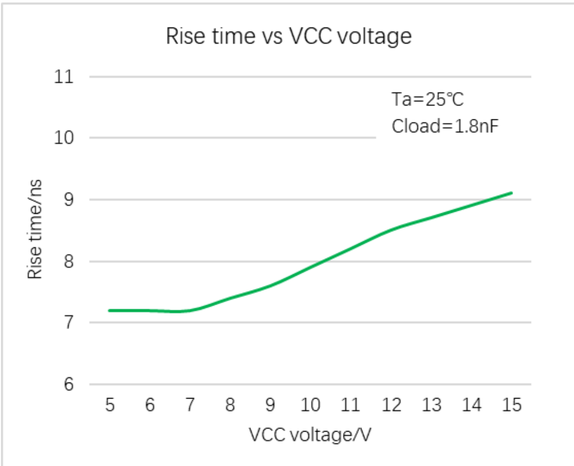
Characteristic plots

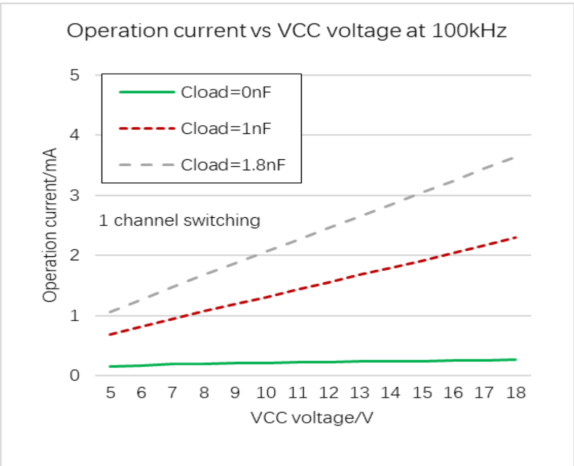
TA=25℃

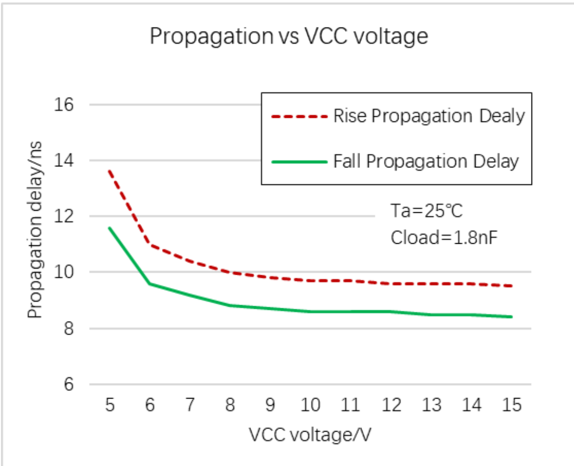


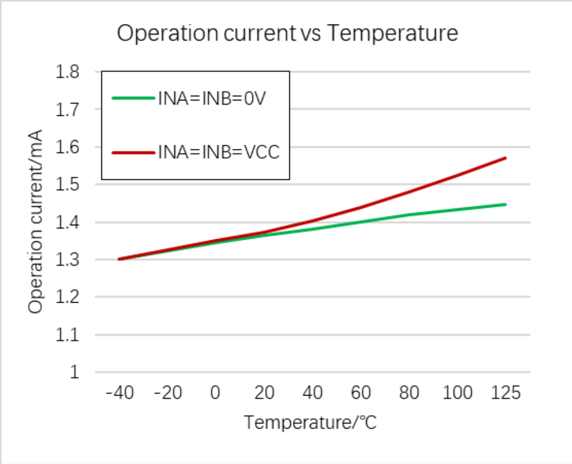


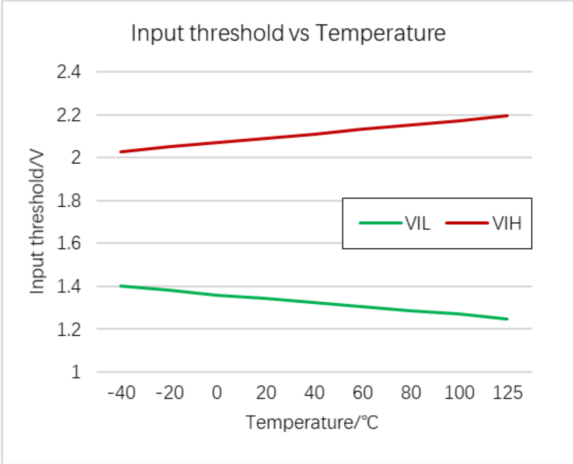












Operation description

Input threshold

Each number of the MX27524 driver family consists of two identical channels that can be used independently at rated current. In the MX27524, channels A and B can be enabled or disabled independently using ENA and ENB, respectively. The EN pins has TTL thresholds for parts with either CMOS and TTL input thresholds. If ENA and ENB are not connected, and internal pull-up resistor enables the driver channels by default. If the channel A and B inputs and outputs are connected in parallel to increase the driver current capacity, ENA and ENB should be connected and driven together. In addition, it is recommended to include an individual gate resistance for each channel to limit the shoot through current possibly happening between the two channels due to variations in propagation delay or input threshold between the two channels.

Under voltage lockout

The MX27524 startup logic is optimized to drive ground-referenced N channel MOSFETs with an under- voltage lockout function to ensure that the IC starts up in an orderly fashion. When VCC is rising, yet below the UVLO level, this circuit holds the output LOW, regardless of the status of the input pins. After the part is active, the supply voltage must drop 0.5V before the part shuts down. This hysteresis helps prevent chatter when low VCC supply voltages have noise from the power switching. This configuration is not suitable for driving high-side P channel MOSFETs because the low output voltage of the driver would turn the P channel MOSFET on with VCC below the UVLO level.

VCC bypass capacitor guidelines

To enable this IC to turn a device on quickly, a local high frequency bypass capacitor, with low ESR and ESL should be connected between the VCC and GND pins with minimal trace length. This capacitor is in addition to the bulk electrolytic capacitance of 10uF to 47uF commonly found on the driver and controller bias circuits. A typical criterion for choosing the value of bypass capacitor is to keep the ripple voltage on the VCC supply to ≤5%. This is often achieved with a value ≥20 times the equivalent load capacitance, defined here as QG/VCC. Ceramic capacitors of 0.1uF to 1uF or larger are common choices, as are dielectrics, such as X5R and X7R with good temperature characteristics and high pulse current capability.

If circuit noise affects normal operation, the value of bypass capacitor may be increased to 50-100 times the equivalent load capacitance, or bypass capacitor may be split into two capacitors. One should be a larger value, based on equivalent load capacitance, and the other a smaller value, such as 1-10nF mounted closest to the VCC and FND pins to carry the higher frequency components of the current pulses.

Layout and connection guidelines

The MX27524 family of gate drivers incorporates fastreacting input circuits, shortage propagation delays, and powerful output stages capable of delivering current peaks over 5A to facilitate voltage transition times from under 10ns to over 150ns. The following layout and connection guidelines are strongly recommended:

●Keep high current output and power ground paths separate logic and enable input signals and signal ground paths. This is especially critical when dealing with TTL-level logic thresholds at driver inputs and enable pins.

●If the inputs to a channel are not externally connected, the internal 400kohm resistor indicated on block diagrams command a low output. In noisy environments, it may be necessary to tie inputs of an unused channel to VDD or GND using short traces to prevent noise from causing spurious output switching.

●Many high speed power circuits can be susceptible to noise injected from their own output or other external sources, possibly causing output re-triggering. These effects can be obvious if the circuit is tested in breadboarding or non-optimal circuit layouts with long input, enable, or output leads. For best results, make connections to all pins as short and direct as possible.

●The MX27524 is compatible with many other industry standard drivers. In single input parts with enable pins, there is an internal 400kohm resistor tied to VDD to enable the driver by default, this should be considered in the PCB layout.

●The turn on and turn off current paths should be minimized, as discussed in the following section

The figure below shows the pulsed gate drive current path when the gate driver is supplying gate charge to turn the MOSFET on. The current is supplied from the local bypass capacitor, and flows through the driver to the MOSFET gate and to ground. To reach the high peak currents possible, the resistance and inductance in the path should be minimized. The localized bypass capacitor acts to contain the high peak current pulses within this driver MOSFET circuit, preventing them from disturbing the sensitive analog circuitry in the PWM controller.

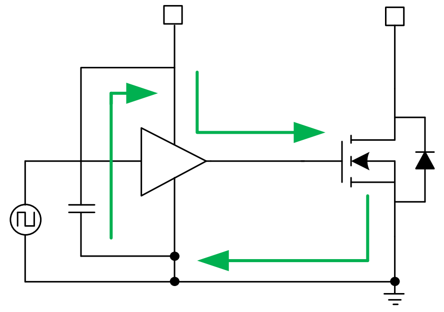


Figure6 Current path for MOSFET turn on

The figure below shows the current path when the gate driver turns the MOSFET off. Ideally, the driver shunts the current directly to the source of the MOSFET in a small circuit loop. For fast turn off times, the resistance and inductance in this path should be minimized.

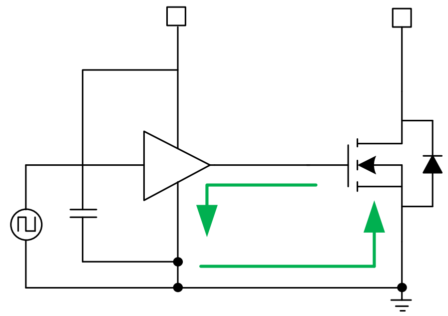


Figure7 Current path for MOSFET turn off

Truth table of logic operation

The MX27524 truth table indicates the operational states using the dual input configuration. If the INA/INB pins is connected to logic high, a disable function is realized, and the driver output remains LOW regardless of the state of the INA/INB pins.

INA/INB	ENA/ENB	VCC	OUTA/B
1	1	>UVLO	1
0	1	>UVLO	0
X	0	>UVLO	0
X	X	<UVLO	0

Operational waveforms

At power up, the driver output remains LOW until the VCC voltage reaches the turn on threshold. The magnitude of the output pulsed rises with VCC until steady state VCC is reached. The operation illustrated in the figure below shows that the output remains LOW until the UVLO threshold is reached, then the output is in phase with the input.

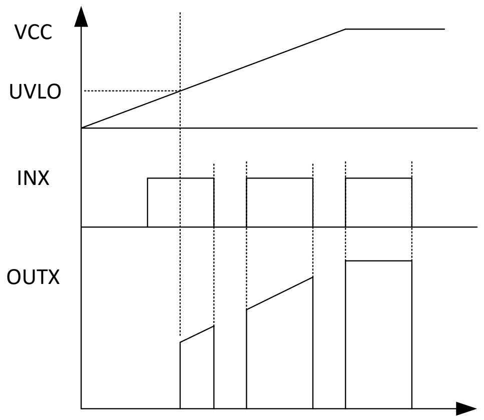


Figure8 The MX27524 start-up waveform

Thermal Guidelines

Gate drivers used to switch MOSFETs, IGBTs and GaNs or SiCs at high frequencies can dissipate significant amounts of power. It is important to determine the drive power dissipation and the resulting junction temperature in the application to ensure that the part is operating within acceptable temperature limits. The total power dissipation in gate driver is the sum of two components, Gate Driving Loss and Dynamic Power Loss.

Gate driving loss P_{GATE} is the most significant power loss result from suppling gate current to switch the load on and off at the switching frequency. The power dissipation that results from driving a power switch at a special gate-source voltage, V_{GS}, with gate charge, Q_G, at switching frequency, F_{SW}, is determined by:

$$P_{GATE} = n \times Q_G \times V_{GS} \times F_{SW}$$

Where n is the number of driver channels in use (1 or 2).

Dynamic power loss P_{DYN} is the power loss resulting from internal current consumption under dynamic operating conditions, including pin pull-up / pull-down resistor. The internal current consumption I_{DYN} can be estimated using the graphs of the typical performance characteristics to determine the current I_{DYN} drawn from VCC under actual operating conditions:

$$P_{DYN} = V_{CC} \times I_{DYN} \times m$$

Where m is the number of driver ICs in use. Note that m is usually be one IC even if in parallel to drive a large load.

Once the power dissipation in the driver is determined, the driver junction rise with respect to circuit board can be evaluated using the following thermal equation, assuming Ψ_{JB} was determined for a similar thermal design:

$$T_J = (P_{GATE} + P_{DYN}) \times \Psi_{JB} + T_{BOARD}$$

Where

T_J is the driver junction temperature;

Ψ_{JB} is thermal characterization parameter relating temperature rise to total power dissipation;

T_{BOARD} is the board temperature in location as defined in the thermal characteristics table.

To give a numerical example, assume for a 12V V_{CC} system, the power MOSFETs which have a total gate charge of 60nC at V_{GS}=12V. Therefore, two devices in parallel would have 120nC gate charge. At a switching frequency of 200kHz, the total power dissipation is:

$$P_{GATE} = 2 \times 120nC \times 12V \times 200kHz = 0.576W$$

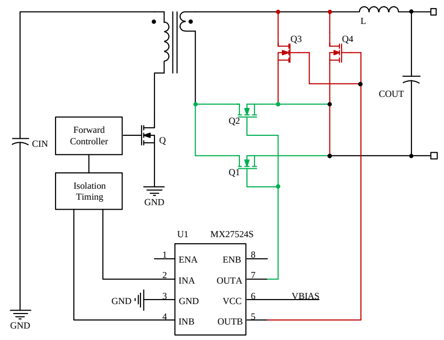
$$P_{DYN} = 12V \times 1.4mA \times 1 = 0.0168W$$

$$P_{TOTAL} = P_{GATE} + P_{DYN} = 0.593W$$

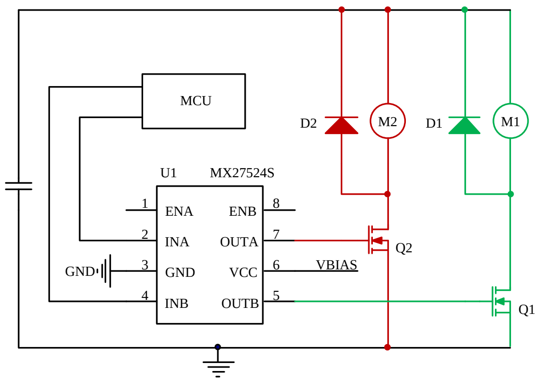
The SOP8 has a junction to board thermal characterization parameter of Ψ_{JB}=42℃/W. In a system application, the localized temperature around the device is a function of the layout and construction of the PCB along with airflow across the surfaces. To ensure reliable operation, the maximum junction temperature of the device must be prevented from exceeding the maximum rating of 150℃, with 80% derating, T_J would be limited to 120℃. Rearranging equation T_J determines the board temperature required to maintain the junction temperature below 120℃.

$$T_{BOARDMAX} = T_J - \Psi_{JB} \times P_{TOTAL}$$

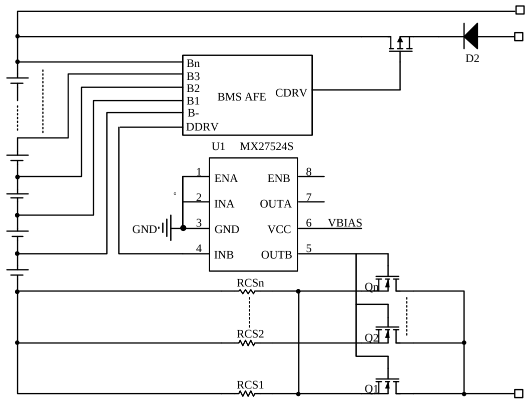
$$T_{BOARDMAX} = 120℃ - 42℃/W \times 0.593W = 95℃$$



High current forward converter with synchronous rectifier

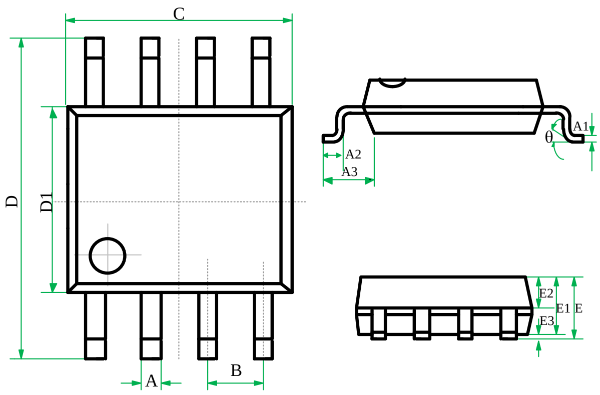


Two brush DC motors driver application



Battery management to drive MOSFETs in parallel

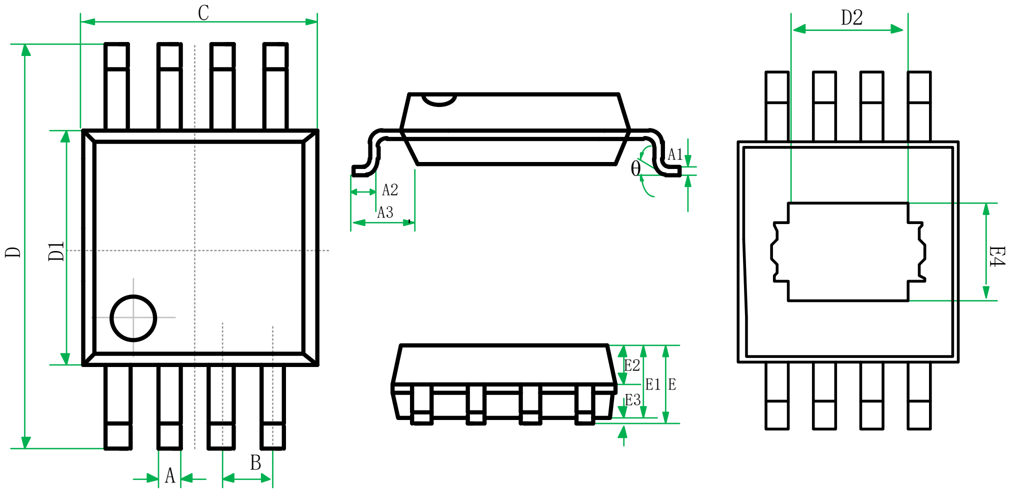
Package information



SYMBOL	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.39	-	0.48	0.0154	-	0.0189
A1	0.21	-	0.28	0.008	-	0.011
A2	0.50	-	0.80	0.020	-	0.031
A3	1.05BSC			0.041BSC		
B	1.27BSC			0.050BSC		
C	4.70	4.90	5.10	0.185	0.193	0.201
D	5.80	6.00	6.20	0.228	0.236	0.244
D1	3.70	3.90	4.10	0.146	0.154	0.161
E	-	-	1.75	-	-	0.069
E1	1.30	1.40	1.50	0.051	0.055	0.059
E2	0.60	0.65	0.70	0.024	0.026	0.028
E3	0.10	-	0.225	0.004	-	0.009
θ	0	-	8°	0	-	8°

SOP8 for MX27524S

Package information eMSOP8



SYMBOL	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.28	0.33	0.38	0.011	0.013	0.015
A1	0.13		0.2	0.005		0.008
A2	0.445	0.546	0.648	0.018	0.021	0.026
A3	0.95BSC			0.037BSC		
B	0.65BSC			0.026BSC		
C	2.9	3.0	3.1	0.114	0.118	0.122
D	4.8	4.9	5.0	0.189	0.193	0.197
D1	2.9	3.0	3.1	0.114	0.118	0.122
E	0.86		1.04	0.034		0.041
E1	0.81		0.91	0.032		0.036
E4	1.246	1.346	1.446	0.049	0.053	0.057
D2	1.55	1.65	1.75	0.061	0.065	0.069
θ	0	-	8°	0		8°

eMSOP8 for MX27524ES