Push-Pull Transformer Driver for Isolated Power Supplies

General description

The MX6501T is a monolithic oscillator or power-driver, specifically designed for small form factor, isolated power supplies in isolated interface applications. The device drives a low profile, center tapped transformer primary from 3.3V to 5V DC power supply. The secondary can be wound to provide any isolated voltage based on transformer turns ratio.

The MX6501T consists of an oscillator followed by a gate drive circuit that provides the complementary output signals to drive the ground referenced N-channel power switches. The internal logic ensures break before make action between the two switches.

The MX6501T is available in a small SOT23 package, and is specified for operation at temperatures from -40℃ to 125℃.

Features

♦ Wide operating input voltage range V_{IN}: 3.3V to 5V

♦ Push-Pull driver for small transformer

♦ Low ripple on rectifier output permits small output capacitors

♦ 5-Pin SOT23-5L

Applications

Industrial automation

Process control

Isolated interface power supply for CAN, RS485, RS422,

Typical application

RS232, SPI, I^2C, Low power LAN

Micro inverter

Battery management system

General information

Ordering information	
Part Number	**Description**
MX6501T	SOT23-5L
MPQ	3000pcs

Package dissipation rating	
Package	**RθJA（℃/W）**
SOT-23 (5)	200

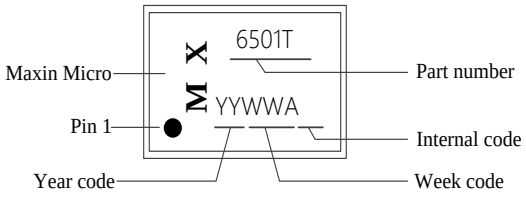
Absolute maximum ratings	
Parameter	**Value**
VCC pin	-0.5 to 7V
V_{D1}, V_{D2}	-0.3 to 36V
I_{D1P}, I_{D2P}	2.4A
Junction temperature	150℃
Storage temperature, Tstg	-50 to 150℃
Leading temperature （soldering,10secs）	260℃
ESD Susceptibility HBM	±2000V

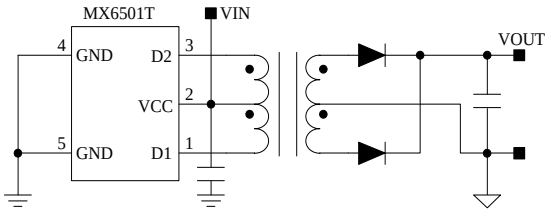
Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional

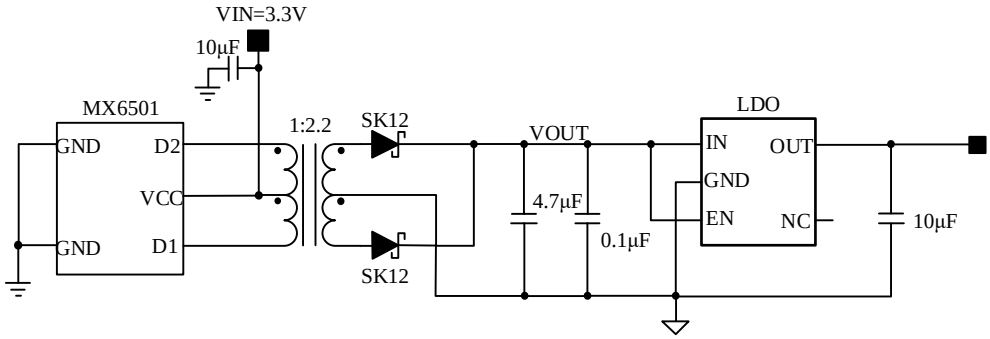
operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

Recommended operating condition	
Symbol	**Range**
VDD	2.25-5.5V
VD1、VD2 switch voltage	30V
I_{D1}, I_{D2}	1A(max)
Operating temperature	-40~125℃
Moisture sensitive level	MSL3

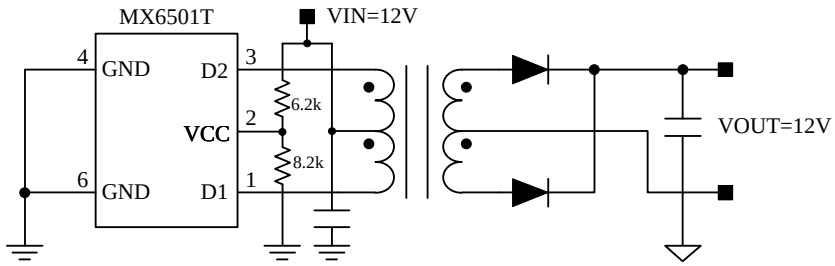
Marking Information





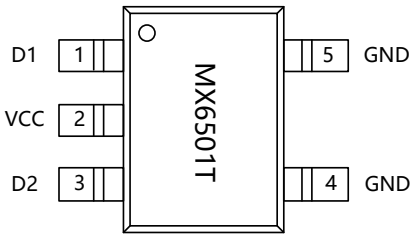


Application 1：3.3V input converter to 5V with LDO



Application 2: 12V input converter to 12V with a resistor divider for VCC supply

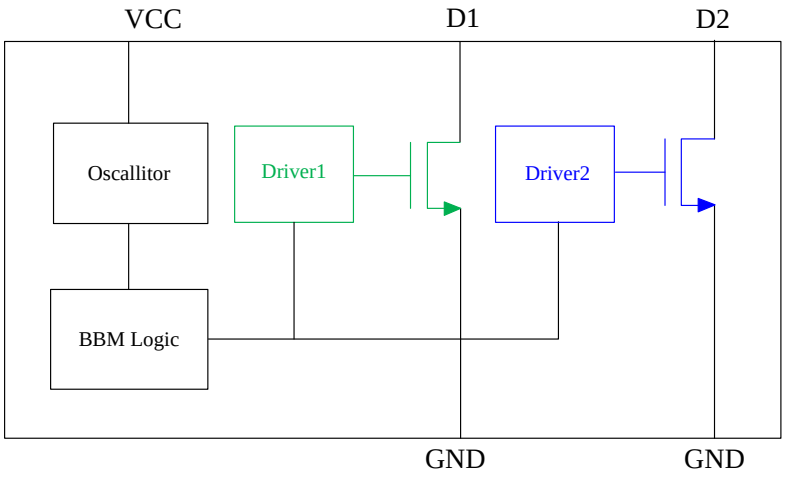
Terminal assignments



Pin information

PIN NO.	PIN name	Description
1	D1	Open Drain output 1. Connect this pin to one end of the push-pull transformer primary side.
2	VCC	Supply voltage input. Connect this pin to the center-tap of the push-pull transformer primary side. Buffer this voltage with a 1uF to 10uF ceramic capacitor.
3	D2	Open Drain output 2. Connect this pin to the other end of the push-pull transformer primary side.
4	GND	Device ground. Connect this pin to the board ground.
5	GND	Device ground. Connect this pin to the board ground.

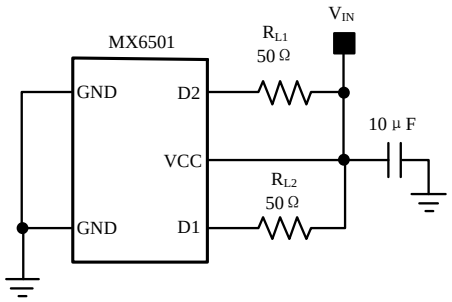
Function Block diagram



Electrical characteristics

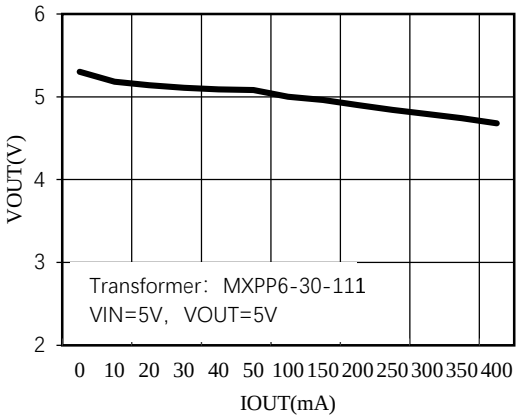
（over full-range of recommended operating conditions, test as following figure, unless otherwise noted）

Symbol	Parameter	Test condition	Min	Typ.	Max	Unit
RON	Switch on resistance	VCC = 3.3V ± 10%, RL = 50Ω	0.1	0.3	0.6	Ω
		VCC = 5V ± 10%, RL = 50Ω	0.1	0.35	0.7	Ω
ICC	Average supply current	VCC = 3.3V ± 10%, no load	0.2	1	1.4	mA
		VCC = 5V ± 10%, no load	0.5	1.5	2.3	mA
$UVLO_{OFF}$	UVLO closure threshold	Positive-going UVLO threshold, RL = 50Ω		2.01	2.25	V
$UVLO_{ON}$	UVLO opening threshold	Negative-going UVLO threshold, RL = 50Ω	1.7	1.83		V
FSW	D1, D2 switching frequency	VCC = 3.3V ± 10%, RL = 50Ω	300	400	500	kHz
		VCC = 5V ± 10%, RL = 50Ω	300	400	500	kHz
Switching Characteristics						
TR_D	D1, D2 output rise time	VCC = 3.3V ± 10%, RL = 50Ω		47		ns
		VCC = 5V ± 10%, RL = 50Ω		48		ns
TF_D	D1, D2 output fall time	VCC = 3.3V ± 10%, RL = 50Ω		20		ns
		VCC = 5V ± 10%, RL = 50Ω		17		ns
TBBM	Break-before-make time	VCC = 3.3V ± 10%, RL = 50Ω		85		ns
		VCC = 5V ± 10%, RL = 50Ω		45		ns

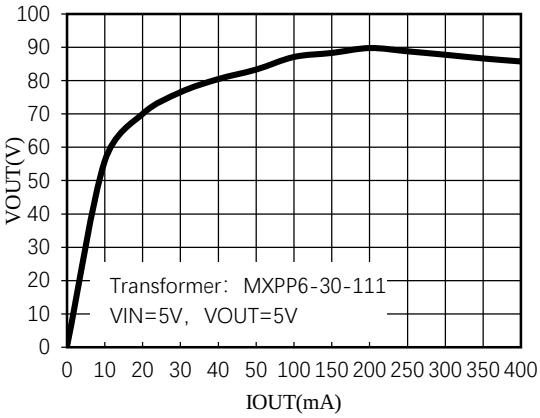


Characteristic plots

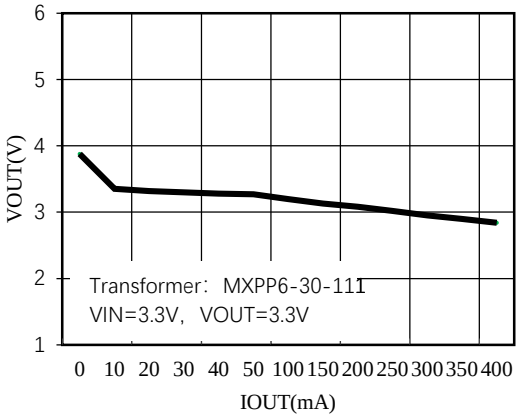
（over full-range of recommended operating conditions, unless otherwise noted）



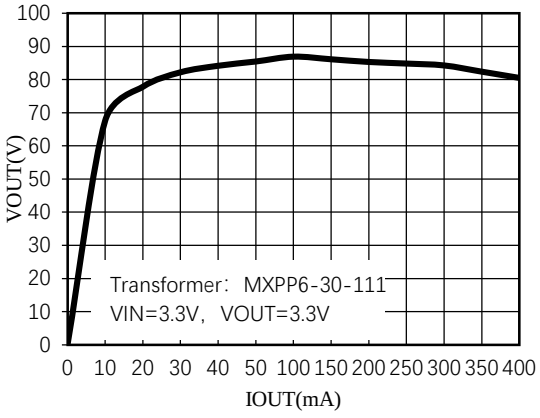
Output voltage vs. load current (5V-5V)



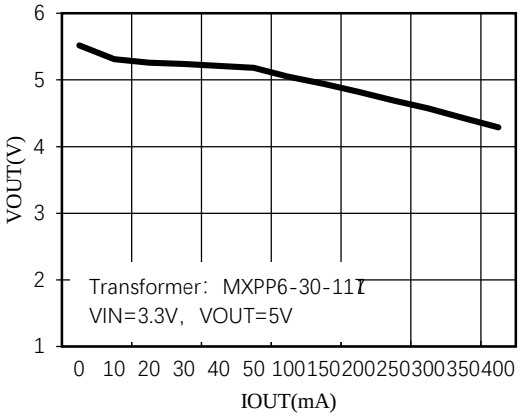
Efficiency vs. load current (5V-5V)



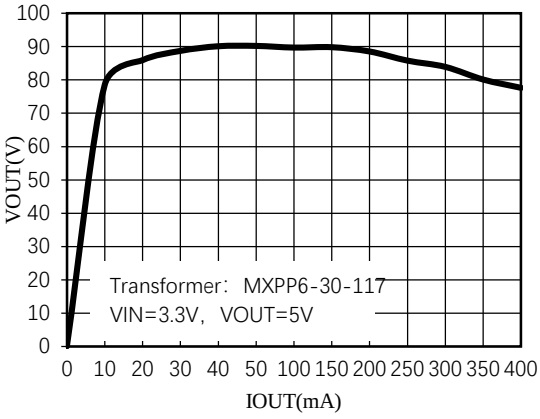
Output voltage vs. load current (3.3V-3.3V)



Efficiency vs. load current (3.3V-3.3V)



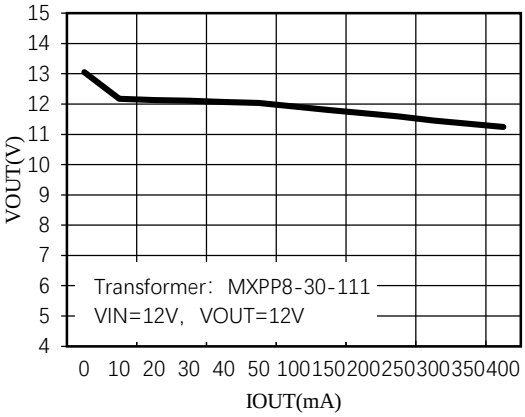
Output voltage vs. load current (3.3V-5V)



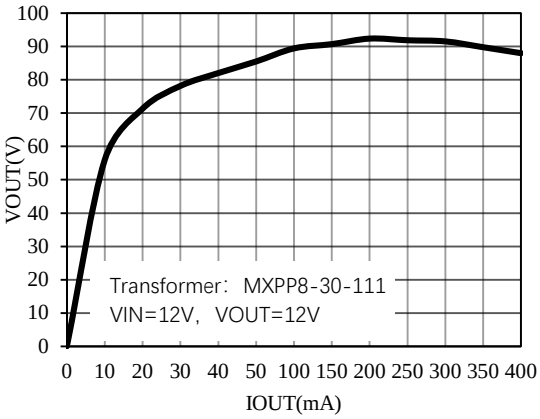
Efficiency vs. load current (3.3V-5V)

V_{IN} = 5V

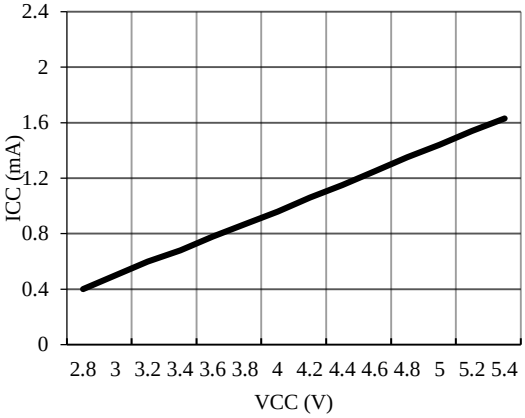
transformer : 760390012



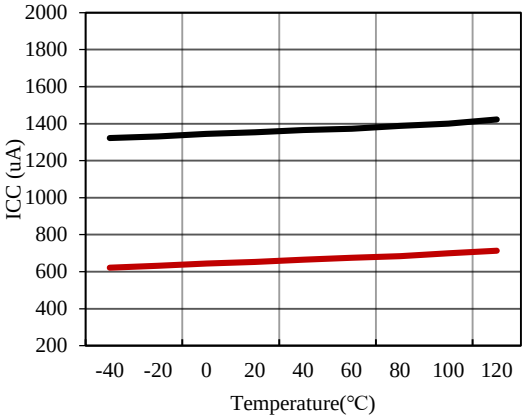
Output voltage vs. load current (10V-10V)



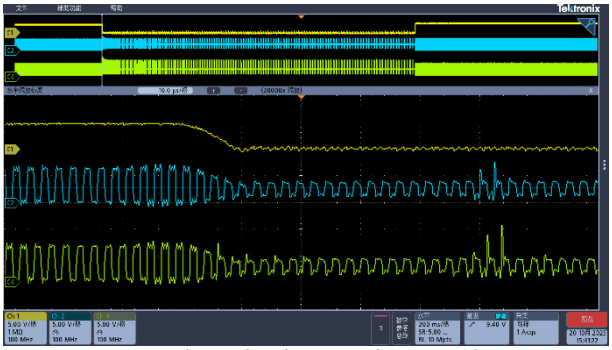
Efficiency vs. load current (10V-10V)



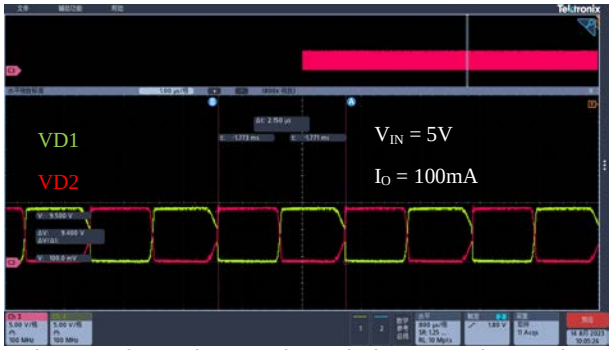
Operating current vs VCC voltage



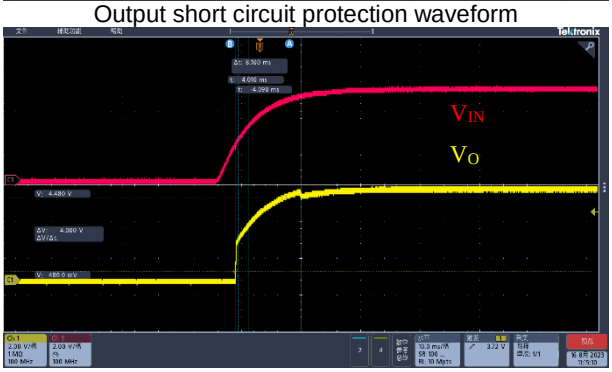
Operating current vs free-air temperature



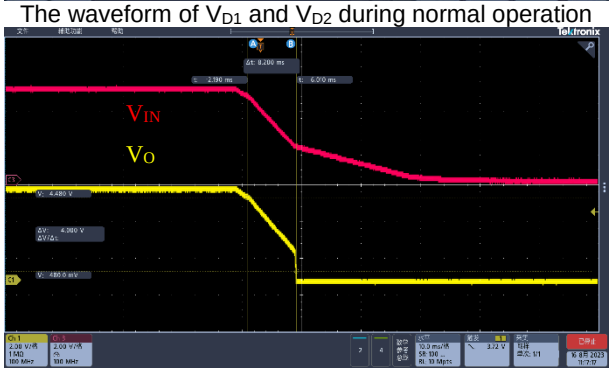
Output short circuit protection waveform



The waveform of V_{D1} and V_{D2} during normal operation



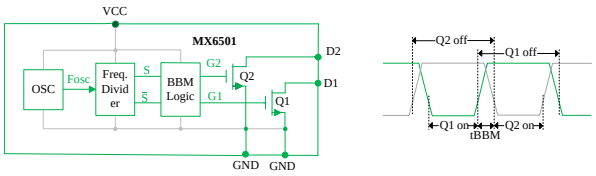
Output rising edge



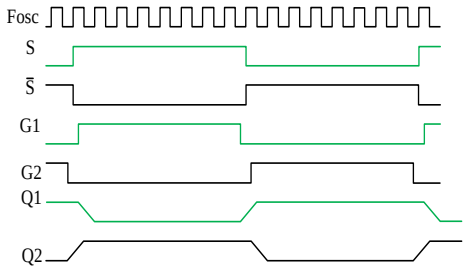
Output falling edge

Operation description

The MX6501T is a transformer driver designed for low cost, small form-factor, isolated DCDC converters utilizing the push-pull topology. The device includes an oscillator that feeds a gate-drive circuit. The gate-drive, comprising a frequency divider and a break-before-make logic, provides two complementary output signals which alternately turn the two output transistors on and off.



The output frequency of the oscillator is divided down by an asynchronous divider that provides two complementary output signals with a 50% duty cycle. A subsequent break-before-make logic inserts a dead time between the high-pluses of the two signals. The resulting output signals, present the gate-drive signals for the output transistors. As shown in the functional block diagram, before either one of the gates can assume logic high, there must be a short period, known as break-before-make time, is required to avoid shorting out both ends of the primary.



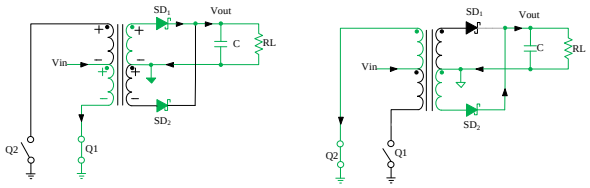
Push-pull converter

Push-pull converters require transformers with center-taps to transfer power from the primary to the secondary as following figure.

When Q1 conducts, V_{IN} drives a current through the lower half of the primary side to ground, thus creating a negative voltage potential at the lower primary end with regards to the V_{IN} potential at the center-tap.

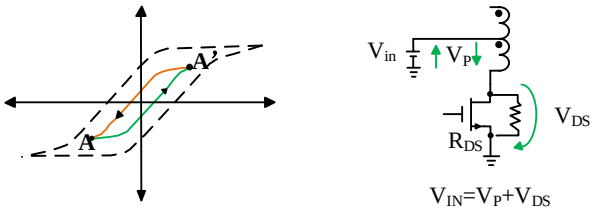
At the same time the voltage across the upper half of the primary is such that the upper primary end is positive with regards to the center-tap in order to maintain the previously established current flow through Q2, which now has turned high-impedance. The two voltage sources, each of which equaling V_{IN}, appear in series and cause a voltage potential at the open end of the primary of $2*V_{IN}$ with regards to ground. Per dot convention the same voltage polarities that occur at the primary also occur at the secondary. The positive potential of the upper secondary end therefore forward biases diode SD_1. The secondary current starting from the upper secondary end flows through SD_1, charges capacitor C, and returns through the load impedance RL back to the center-tap.

When Q2 conducts, Q1 goes high-impedance and the voltage polarities at the primary and secondary reverse. Now the lower end of the primary presents the open end with a $2*V_{IN}$ potential against ground. In this case SD_2 is forward biases while SD_1 is reverse biases and current flows from the lower secondary end through SD_2, charging the capacitor and returning through the load to the center-tap.



Core magnetization

The following figure shows the ideal magnetizing curve for a push-pull converter with B as the magnetic flux density and H is the magnetic field strength. When Q1 conducts the magnetic flux is pushed from A to A', and when Q2 conducts the magnetic flux is pulled back from A' to A. The difference in magnetic flux and thus in flux density is proportional to the product of the primary voltage, V_P, and the time, Ton, it is applied to the primary:



This volt-seconds product is important as it determines

the core magnetization during each switching cycle. If the V-t products of both phases are not identical, an imbalance in flux density swing an offset from the origin of the B-H curve. If balance is not restored, the offset increases with each following cycle and the transformer slowly creeps toward the saturation region.

Fortunately, due to the positive temperature coefficient of the on-resistance of MOSFET, the output FETs of the MX6501T have a self-correcting effect on V-t imbalance. In the case of a slightly longer on-time, the prolonged current flow through a FET gradually heats the transistor which leads to an increase in on resistance. The higher resistance then causes the drain to source voltage, V_{DS}, to rise. Because the voltage at the primary is the difference between the constant input voltage, V_{IN}, and the voltage drop across the MOSFET, $V_P = V_{IN} - V_{DS}$, V_P is gradually reduced and V-t balance restored.

Startup mode

When the supply voltage at V_{CC} ramps up to 2.25V typical, the internal oscillator starts operating at a start frequency of 400kHz. The output stage begins switching but the amplitude of the drain signals at D1 and D2 has not reached its full maximum yet.

Operating Mode

When the supply voltage has reached its nominal value ±10% the oscillator is fully operating. However variations over supply voltage and operating temperature can vary the switching frequencies at D1 and D2 400kHz for V_{CC} = 3.3V ± 10% and V_{CC} = 5V ± 10%.

Off mode

The MX6501T is deactivated by reducing V_{CC} to 0V. In this state both drain outputs, D1 and D2, are high impedance.

Typical Application

MX6501T Drive Capability

The MX6501T transformer diver is designed for low power push-pull converters with input and output voltages in the range of 2.25V to 5.5V. While converter designs with higher output voltages are possible, care must be taken that higher turns ratio don't lead to primary currents that exceed the MX6501T specified current limits.

MX6501T does not have soft start, internal current limit, or thermal shutdown features. Therefore to address possible unregulated or large currents, there is a limit to the maximum capacitive load that can be connected to an MX6501T system. Loads exceeding 5uF appear as short circuits to MX6501T during power up and may affect the device's long-term reliability. When using MX6501T, it is recommended to keep capacitive loads below 5uF or incorporate LDOs with low short circuit current limits or soft start features to ensure excessive current is not drawn from MX6501T.

LDO selection

The minimum requirements for a suitable low dropout regulator are:

Its current drive capability should slightly exceed the specified load current of the application to prevent the LDO from dropping out of regulation. Therefore for a load current of 100mA, choose a 100mA to 150mA LDO. While regulators with higher drive capabilities are acceptable, they also usually possess higher dropout voltages that will reduce overall converter efficiency.

The internal dropout voltage, V_{DO}, at the specified load current should be as low as possible to maintain efficiency. For a low cost 150mA LDO, a V_{DO} of 150mV at 100mA is common. Be-aware however, that this lower value is usually specified at room temperature and can increase by a factor of 2 over temperature, which in turn will raise the required minimum input voltage.

The required minimum input voltage preventing the regulator from dropping out of line regulation is given with:

$$V_{I\text{-}MIN} = V_{DO\text{-}MAX} + V_{O\text{-}MAX}$$

This means in order to determine V_I for worst-case condition, the user must take the maximum values for V_{DO} and V_O specified in the LDO datasheet for rated output current and add them together. Also specify that the output voltage of the push-pull rectifier at the specified load current is equal or higher than V_{I_MIN}. if it is not, the LDO will lose line-regulation and any variations at the input will pass straight through to the output. Hence below V_{I_MIN} the output voltage will follow the input and the regulator behaves like a simple conductor.

The maximum regulator input voltage must be higher than the rectifier output under no-load. Under this condition there is no secondary current reflected back to the primary, thus making the voltage drop across R_{DS_ON} negligible and allowing the entire converter input voltage to drop across the primary. At this point the secondary reaches its maximum voltage of

$$V_{S\text{-}max} = V_{IN\text{-}max} \times n$$

With V_{IN_MAX} as the maximum converter input voltage and n as the transformer turns ratio. Thus to prevent the LDO from damage the maximum regulator input voltage must be higher than V_{S_MAX}. The following table lists the maximum secondary voltage for various turns ratios commonly applied in push-pull converters with 100mA output drive.

Push-pull converter				LDO
Configuration	**VIN-max [V]**	**Turns-ratio**	**VS-max [V]**	**VI-max [V]**
3.3V VIN to 3.3V VOUT	3.6	1.5 ± 3%	5.6	6 ~ 10
3.3V VIN to 5V VOUT	3.6	2.2 ± 3%	8.2	10
5V VIN to 5V VOUT	5.5	1.5 ± 3%	8.5	10

Diode selection

A rectifier diode should always possess low forward voltage to provide as much voltage to the converter output as possible. When used in high frequency switching applications, such as the MX6501T however, the diode must also possess a short recovery time. Schottky diodes meet both requirements and are therefore strongly recommended in push-pull converter designs.

Capacitor selection

The capacitors in the converter circuit in the following figure are multi-layer ceramic chip capacitors.

As with all high speed CMOS ICs, the MX6501T requires a bypass capacitor in the range of 10nF to 100nF.

The input bulk capacitor at the center-tap of the primary supports large current into the primary during the fast switching transients. For minimum ripple make this capacitor 1uF to 10uF. In a 2-layers PCB design with a dedicated ground plane, place this capacitor close to the primary center-tap to minimize trace inductance. In a 4-layers PCB design with low inductance reference planes for ground and V_{IN}, the capacitor can be placed at the supply entrance of the board. To ensure low inductance paths use two vias in parallel for each connection to a reference plane or to the primary center-tap.

The bulk capacitor at the rectifier output smooth the output voltage. Make this capacitor 1uF to 10uF.

The small capacitor at the regulator input is not necessarily required. However, good analog design practice suggests, using a small value of 47nF to 100nF improves the regulator's transient response and noise rejection.

The LDO output capacitor buffers the regulated output for the subsequent isolator and transceiver circuitry. The choice of output capacitor depends on the LDO stability requirements specified in the datasheet. However, in most cases, allow ESR ceramic capacitor in the range of 4.7uF to 10uF will satisfy these requirements.

Transformer selection

V-t product calculation

To prevent a transformer from saturation its V-t product must be greater than the maximum V-t product applied by MX6501T. The maximum voltage delivered by the MX6501T is the nominal converter input plus 10%. The maximum time this voltage is applied to the primary is half the period of the lowest frequency at the specified input voltage. Therefore, the transformer's minimum V-t product is determined by the following function:

$$Vt_{min} \geq V_{IN\text{-}max} \times T_{max} / 2 = V_{IN\text{-}max} / (2 \times f_{min})$$

Common V-t values for low power center-tapped transformers range from 22Vus to 150Vus with typical foot prints of 10mm*12mm. However, transformers specifically designed for PCMCIA applications provides as little as 11Vus and come with a significantly reduced footprint of 6mm*6mm only.

While Vt-wise all of these transformers can be driven by the MX6501T, other important factors such as isolation voltage, transformer wattage, and turns ratio must be considered before making the final decision.

Turns ration estimate

Assume the rectifier diodes and linear regulator has been selected. Also, it has been determined that the transformer chosen must have a V-t product of at least

11Vus. However, before searching the manufacturer websites for a suitable transformer, the user still needs to know its minimum turns ratio that allows the push-pull converter to operate flawlessly over the specified current and temperature range. This minimum transformation ratio is expressed through the ratio of minimum secondary to minimum primary voltage multiplied by a correction factor that takes the transformer's typical efficiency of 97% into account:

$$V_{P\text{-}min} = V_{IN\text{-}min} - V_{DS\text{-}max}$$

V_{S_min} must be large enough to allow for a maximum voltage drop, V_{F_max}, across the rectifier diode and still provide sufficient input voltage for the regulator to remain in regulation. From the LDO selection section, this minimum input voltage is known and by adding V_{F_max} gives the minimum secondary voltage with the following function:

$$V_{S\text{-}min} = V_{F\text{-}max} + V_{DO\text{-}max} + V_{O\text{-}max}$$

Then calculating the available minimum primary voltage, V_{P_min}, involves subtracting the maximum possible drain-source voltage of the MX6501T, V_{D_MAX}, form the minimum converter input voltage V_{IN_MIN}:

$$V_{P\text{-}min} = V_{IN\text{-}min} - V_{DS\text{-}max}$$

V_{DS_MAX} however, is the product of the maximum R_{DSON} and I_D values for a given supply specified in the MX6501T datasheet:

$$V_{DS\text{-}max} = R_{DS\text{-}max} \times I_{Dmax}$$

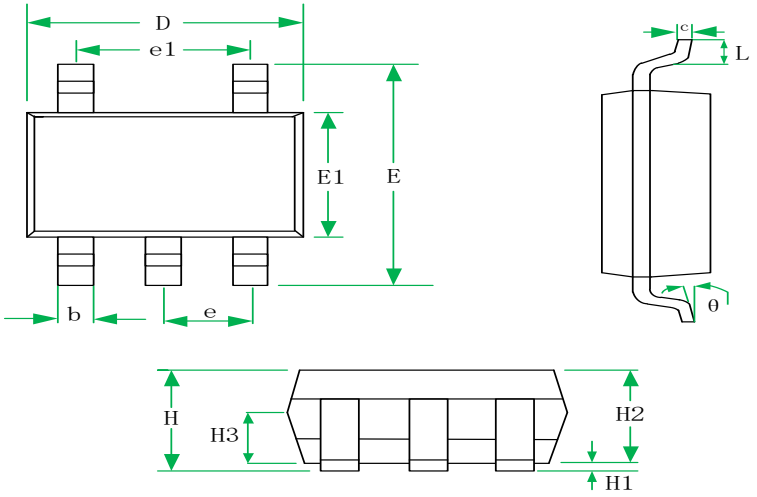
Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 2.5V and 5V nominal. This input supply must be regulated within ± 10%. If the input supply is located more than a few inches from the SN6501 a 0.1μF by-pass capacitor should be connected as possible to the device V_{CC} pin, and a 10μF capacitor should be connected close to the transformer center-tap pin.

Layout Guidelines

- The V_{IN} pin must be buffered to ground with a low-ESR ceramic bypass-capacitor. The recommended capacitor value can range from 1μF to 10μF. The capacitor must have a voltage rating of 10V minimum and a X5R or X7R dielectric.
- The optimum placement is closest to the V_{IN} and GND pins at the board entrance to minimize the loop area formed by the bypass-capacitor connection, the V_{IN} terminal, and the GND pin.
- The connections between the device D1 and D2 pins and the transformer primary endings, and the connection of the device V_{CC} pin and the transformer center-tap must be as close as possible for minimum trace inductance.
- The connection of the device V_{CC} pin and the transformer center-tap must be buffered to ground with a low-ESR ceramic bypass-capacitor. The recommended capacitor value can range from 1μF to 10μF. The capacitor must have a voltage rating of 16V minimum and a X5R or X7R dielectric.
- The device GND pins must be tied to the PCB ground plane using two vias for minimum inductance.
- The ground connections of the capacitors and the ground plane should use two vias for minimum inductance.
- The rectifier diodes should be Schottky diodes with low forward voltage in the 10mA to 100mA current range to maximize efficiency.
- The V_{OUT} pin must be buffered to ISO-Ground with a low-ESR ceramic bypass-capacitor. The recommended capacitor value can range from 1μF to 10μF. The capacitor must have a voltage rating of 16V minimum and a X5R or X7R dielectric.

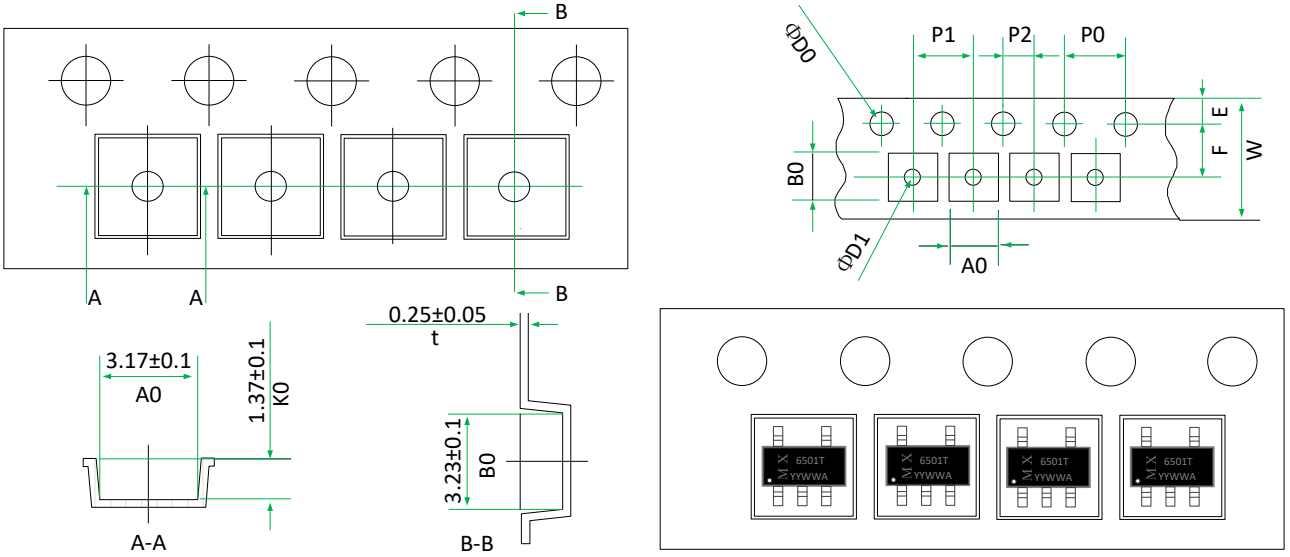
Package information



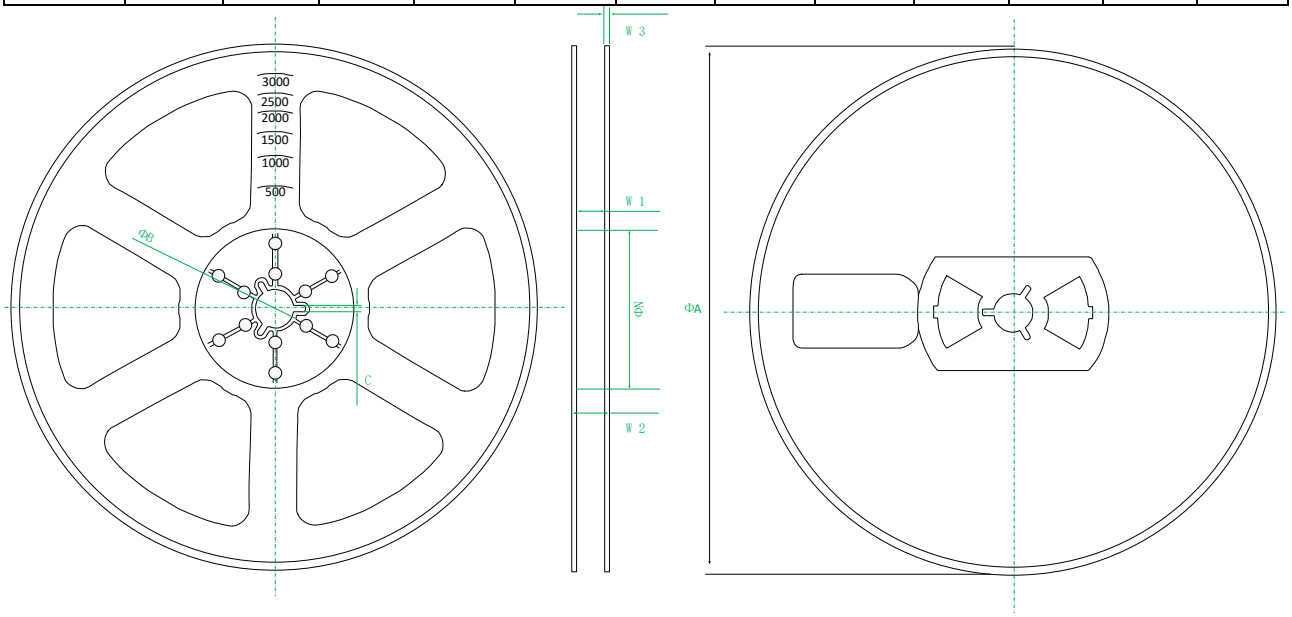
SYMBOL	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
H	1.07		1.25	0.042		0.049
H1	0.02	0.06	0.10	0.001	0.002	0.004
H2	1.05	1.10	1.15	0.041	0.043	0.045
H3	0.60	0.65	0.70	0.024	0.026	0.028
b	0.30	0.40	0.50	0.012	0.016	0.020
c	0.102	0.152	0.202	0.004	0.006	0.008
D	2.82	2.92	3.02	0.111	0.115	0.119
E	2.65	2.80	2.95	0.104	0.110	0.116
E1	1.50	1.60	1.70	0.059	0.063	0.067
e	0.95BSC			0.037BSC		
e1	1.90BSC			0.075BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
θ	0		8°	0		8°

SOT23-5 for MX6501T

Tape and Reel Information (unit in mm)



Symbol	W	E	F	ΦD0	ΦD1	P0	P1	P2	A0	B0	K0	t
MAX	8.10	1.85	3.55	1.60	1.25	4.10	4.10	2.05	3.27	3.33	1.47	0.30
MIN	7.90	1.65	3.45	1.40	1.0	3.90	3.90	1.95	3.07	3.13	1.27	0.20



Symbol	ΦA	ΦN	ΦB	C	W1	W2	W3
MAX	180	56	13.5	2.50	9.9	12	1.8
MIN	176	52	13.0	1.90	8.4		1.0

Version update record:

V10 The original version （preliminary）

V11 The released version